Amendment

Amendment to Specification

Please amend the specification as shown below.

Paragraph on page 2, starting at line 13:

a1

However, as manufacturing techniques improve, the channel length of transistors is typically reduced, which, in turn, may increase the sub-threshold leakage of the transistors. Consequently, the clamping devices may become a significant source of leakage current while the integrated circuit is in operation. Thus, there is a continuing need for better ways to provide charge protection to an integrated circuit that have reduced leakage currents.

Paragraph on page 4, starting at line 16:

a2

Embodiment 100 here includes an integrated circuit 10 that may comprise, for example, a microprocessor, a digital signal processor, a microcontroller, or the like. However, it should be understood that only a portion of integrated circuit 10 is included in FIG. 1 and that the scope of the present invention is not limited to these examples. Integrated circuit 10 may comprise core logic 20 that may include transistors that [are] perform the instructions or operations executed by integrated circuit 10.

Paragraph on page 6, starting at line 16:

a3 cnt.

Integrated circuit 10 may also optionally comprise timer or delay units that may be used to enable the operation of clamping transistor 50 and a biasing transistor 31. For example, transistors 35-36 may act as an inverter that enables biasing transistor 31 if there is a voltage potential stored on capacitor 40 (e.g.,

a3 cancel'd.

during an ESD event). Transistors 33-34 and 37-38 may act as two inverters in series that enable the operation of clamping transistor 50. However, clamping transistor 50 may be substantially enabled after biasing transistor 31 due to the extra inverter in the path of the enabling signal. As explained in more detail below, biasing transistor 31 may be desirable so to offset or compensate the reverse biasing of clamping transistor 50 that may occur while [integrated in] under normal operation (e.g. [integrated circuit if] performing its intended operations such as executing instructions, storing data, processing data, etc.). This may allow transistor 50 to conduct more current during an ESD event.

Paragraph on page 8, starting at line 9:

a4

When integrated circuit experiences an ESD event (e.g. excess charge is present on the power supply voltage potential line, capacitor 40 and the inverter provided by transistors 35-36 may enable biasing transistor. For example, the excessive charge may, at least in part, result in a high voltage potential on the gate terminal of biasing transistor 31. This, in turn, may cause biasing transistor 31 to conduct so that the power supply voltage potential, Vcc, may be applied to the bulk region of clamping transistor 50. This may be desirable to offset or compensate for the reverse biasing effect provided by resistive element 30 so that clamping transistor 50 may have a lower threshold voltage. Consequently, the charge protection device may provide a path to ground for the excessive charge that has lower impedance than the devices in core logic 20 [50]. Consequently, the charge may be dissipated without causing any damage to core logic 20 [50].

Paragraph on page 9, starting at line 7:

FIG. 2 is provided to illustrate an example of [for] the dense arrangement of biasing transistor 31, although the scope of the present invention is not limited to this particular example. It should be understood that in alternative embodiments, the transistors shown in the figures may have opposite polarity (e.g., n-channel devices instead of p-channel devices, etc.) and the scope of the present invention is [in] not limited to a particular substrate material as alternatives such as semiconductor-on-insulator (SOI) may also be used.

a5

Paragraph on page 9, starting at line 14:

FIG. 2 illustrates a cross-sectional view of biasing transistor along with a corresponding top view of the layout structure. Biasing transistor 31 may be formed in a p substrate 210 and include a gate structure 215 that partially overlaps both p substrate 210 and an n-well region 200. Optionally, the charge protection device, such as clamping transistor 50 may also be formed in n-well region 200 to reduce the amount of interconnect use to couple biasing transistor 31 to clamping transistor 50. This arrangement may protect the gate of transistor 21 [21] from the substantially higher voltage potential on its drain node.

Paragraph on page 10, starting at line 19:

a6 cont.

Reverse body bias on one of the transistors of the charge protection device (e.g., transistor 350) may reduce the leakage current through transistor 350 [may be reduced]. Since transistor 351 is in series with transistor 350, the leakage current through transistor 351 may be reduced the same or similar amount. Having multiple transistors in series to provide the charge protection device may be desirable because the combination of transistors in series may allow the charge

a6 cncl'd

protection device to protect for ESD events on nodes with higher voltage potentials (e.g., input/output voltages).

Paragraph on page 11, starting at line 13:

a7

As shown in FIG. 4, a plurality of transistors 410 may be used to provide a voltage divider 411. Voltage divider 411 may be used to provide an output voltage potential that is a fraction of the power supply voltage potential, Vcc. The output voltage potential may be provided to a voltage buffer 430. Voltage buffer 430 may be provided with transistors 420-421 and may be used to amplify or drive a voltage potential to the gate terminal of clamping transistor 450. This particular embodiment may also comprise inverters 460-464 that may be use to delay or time when clamping transistors 450-451 are enabled so that they may provide a low impedance path for excessive charge during an ESD event. As shown in FIG. 4, the source terminal of transistor 450 may float while the bulk region of transistor 450 is connected to the power supply voltage potential. Consequently, transistor 450 may be reverse body biased when there is no ESD event. It should be understood that it may be desirable, in alternative embodiments, to remove transistor 32, resistor 55, and capacitor 40 in an effort to reduce the size of the overall circuit. Although the scope of the present invention is not limited in this respect, some embodiments may include a diode (e.g. diode 360 of FIG. 3 or diode 43 of FIG. 4), a capacitor (e.g. capacitor 320 of FIG. 3 or capacitor 41 of FIG. 4, and/or a resistor (e.g. resistor 317 of FIG. 3).